

FIG. 1

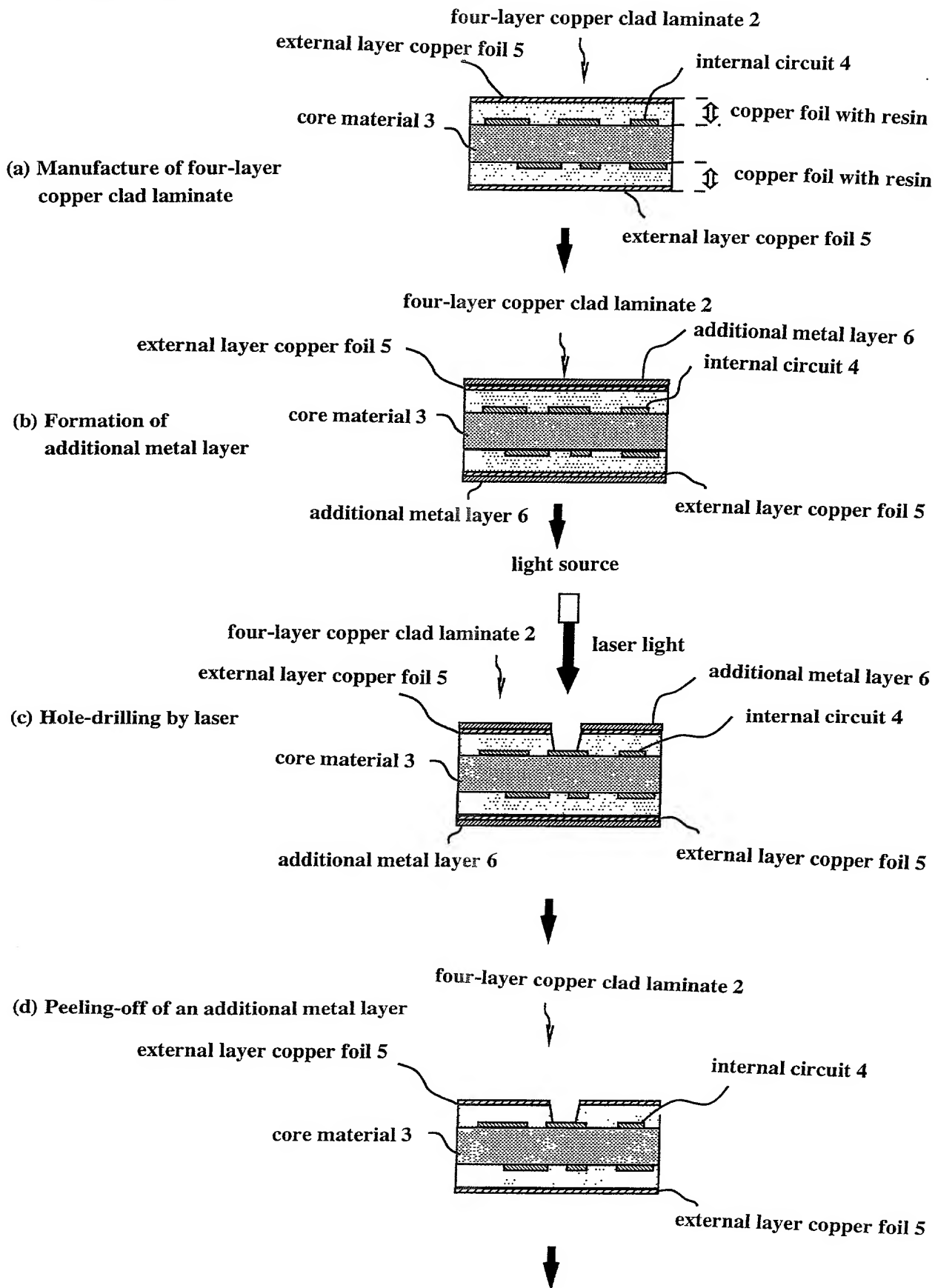


FIG. 2

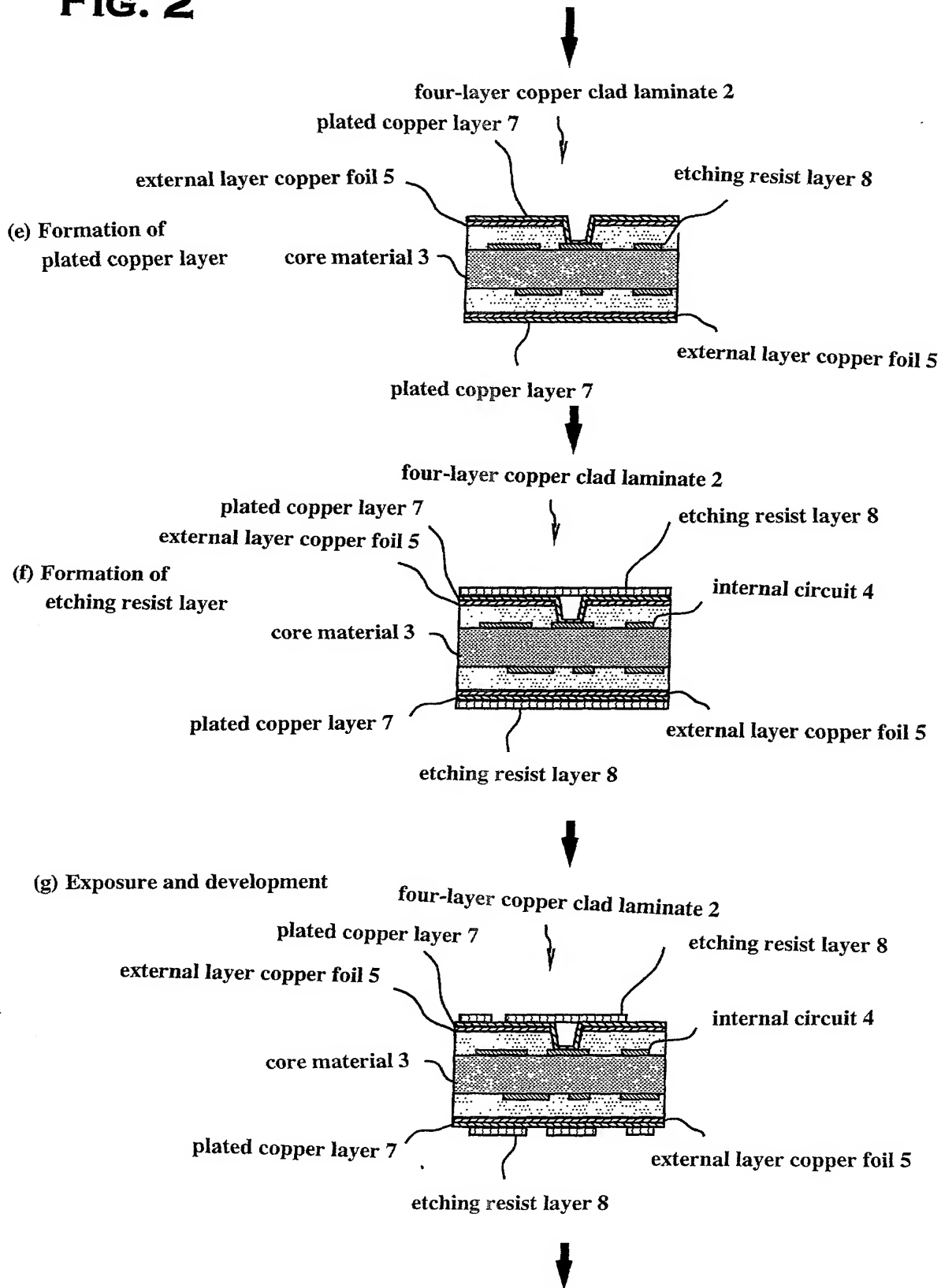
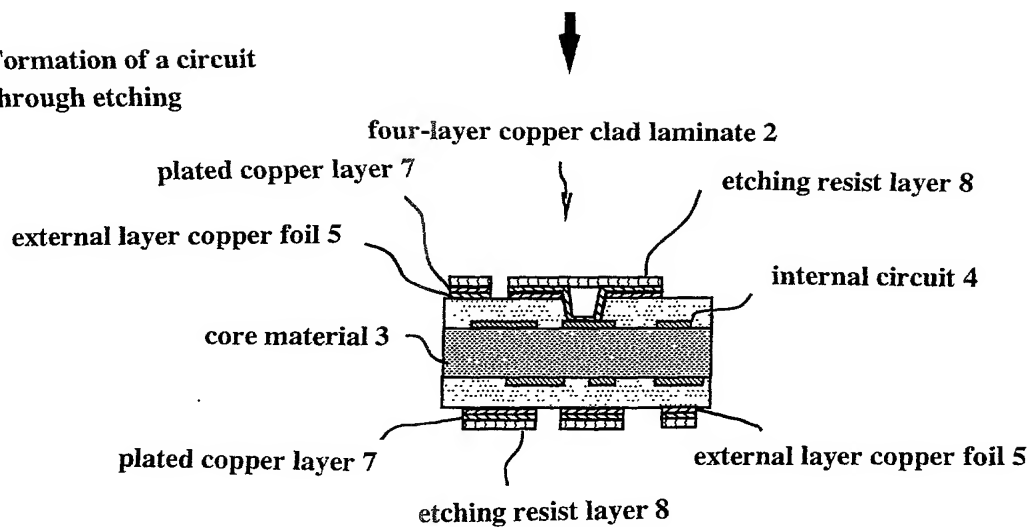


FIG. 3

(h) Formation of a circuit through etching



(i) Peeling-off of etching resist layer

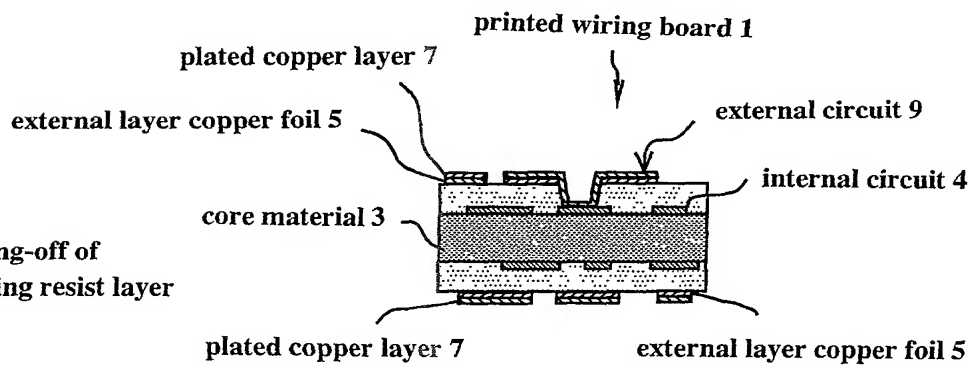


FIG. 4

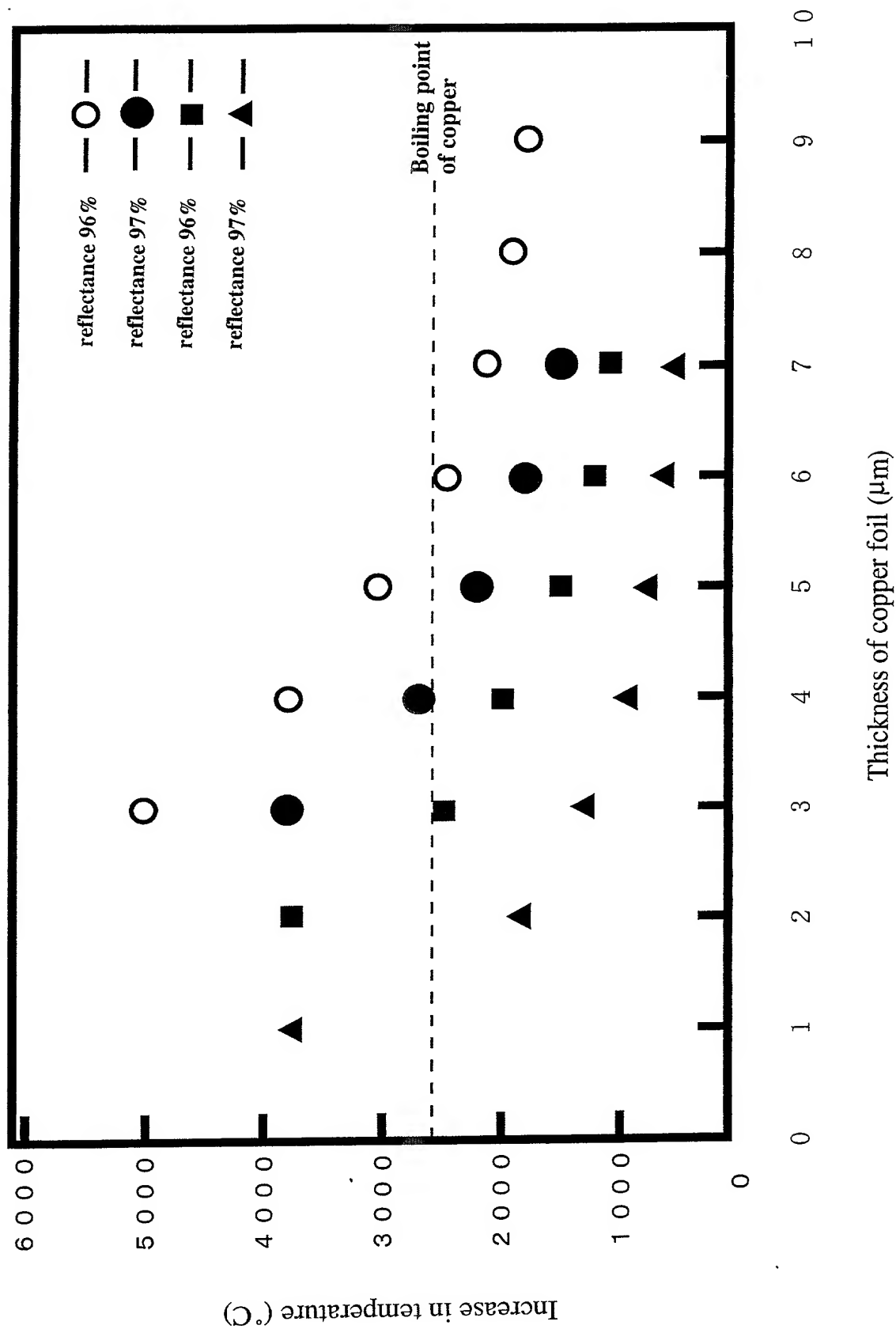


FIG. 5

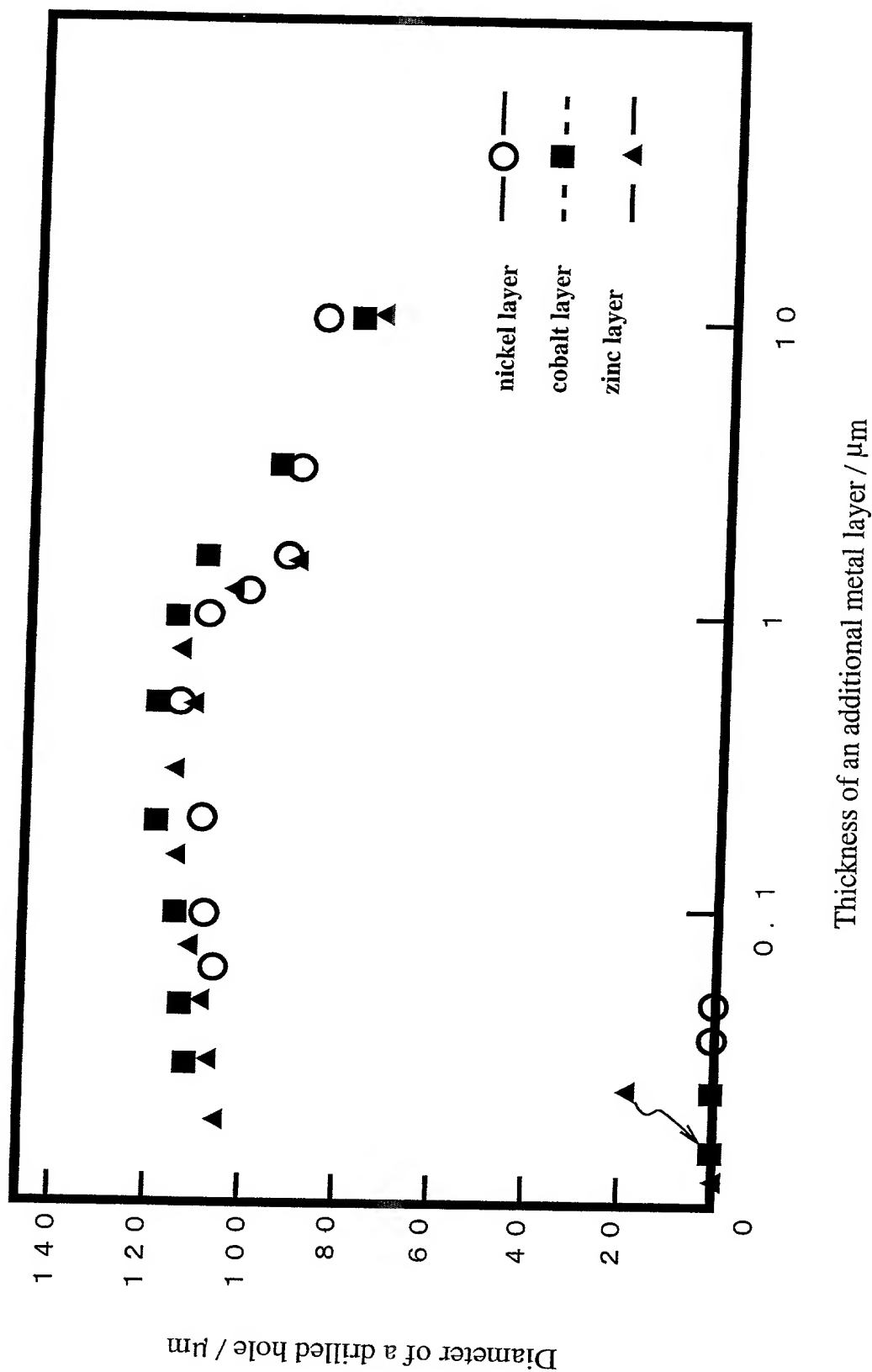


FIG. 6

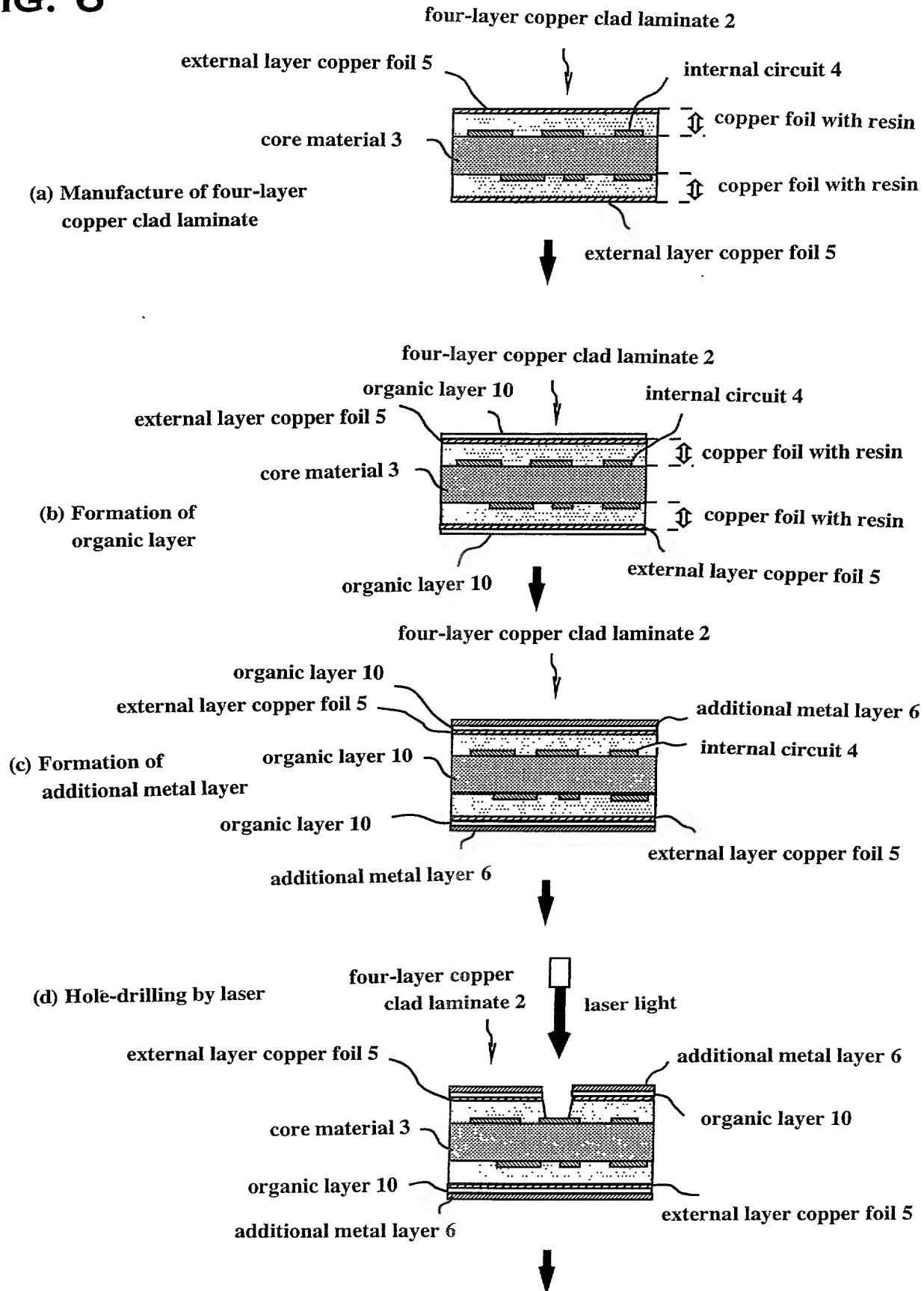


FIG. 7

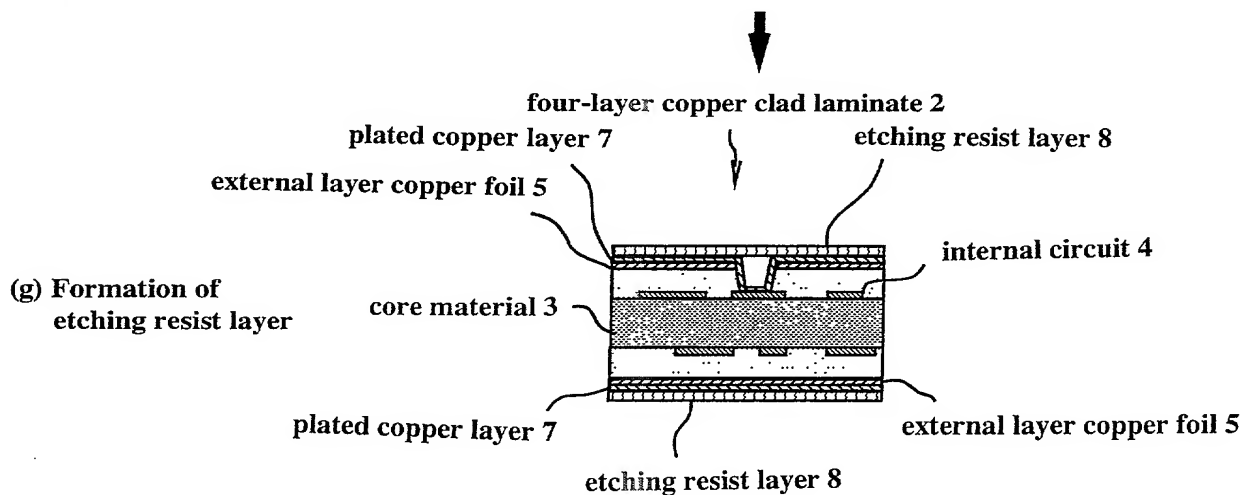
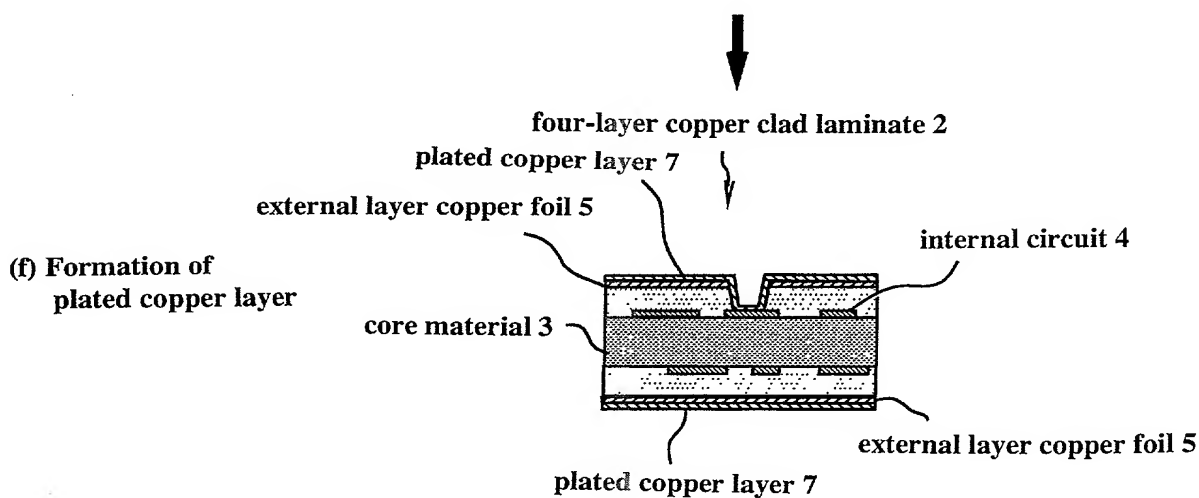
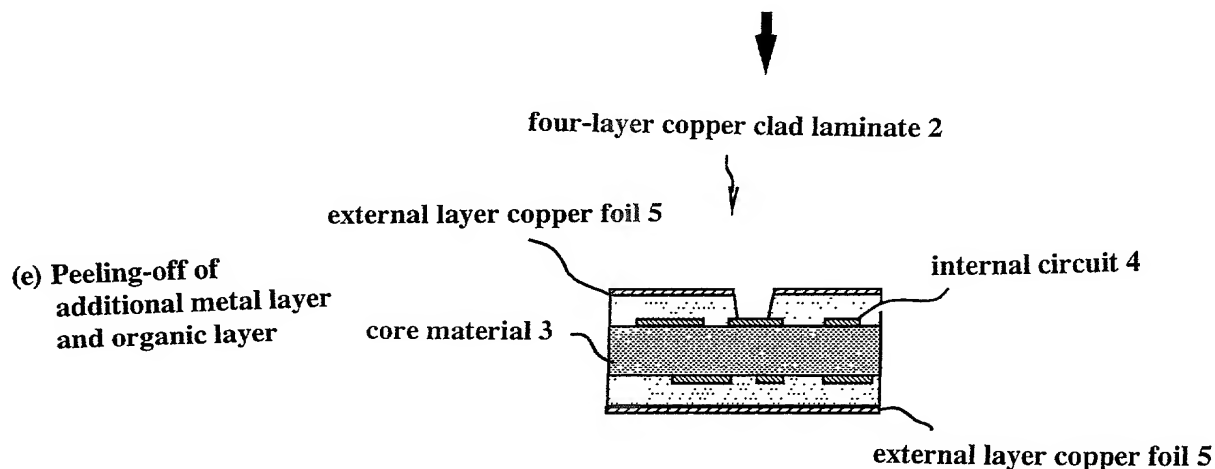
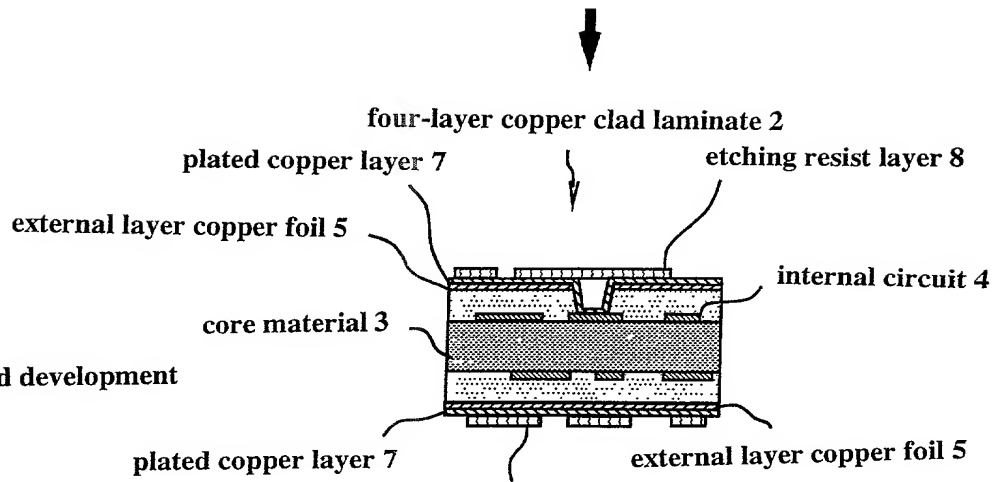
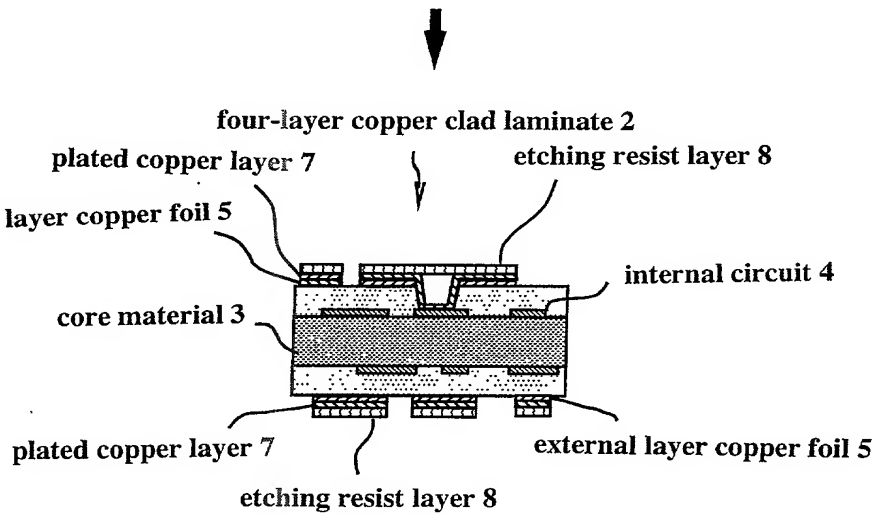


FIG. 8

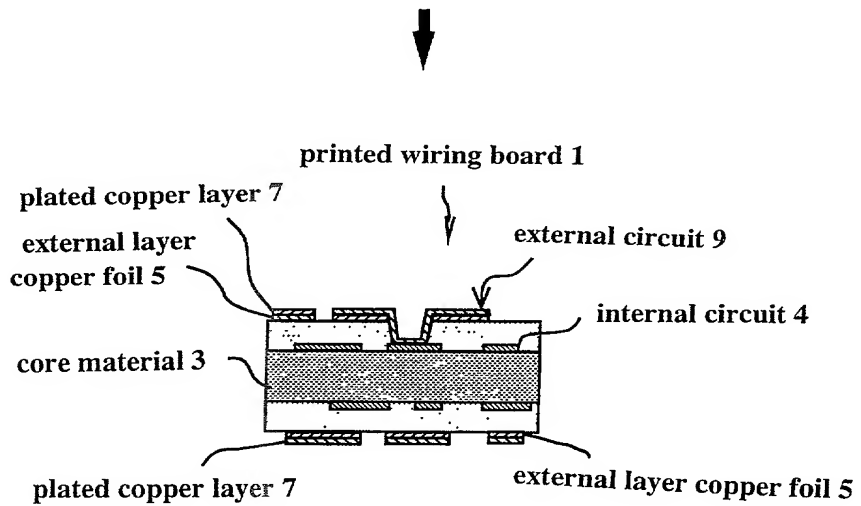
(h) Exposure and development



(i) Formation of a circuit through etching



(j) Peeling-off of etching resist layer



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FIG. 9

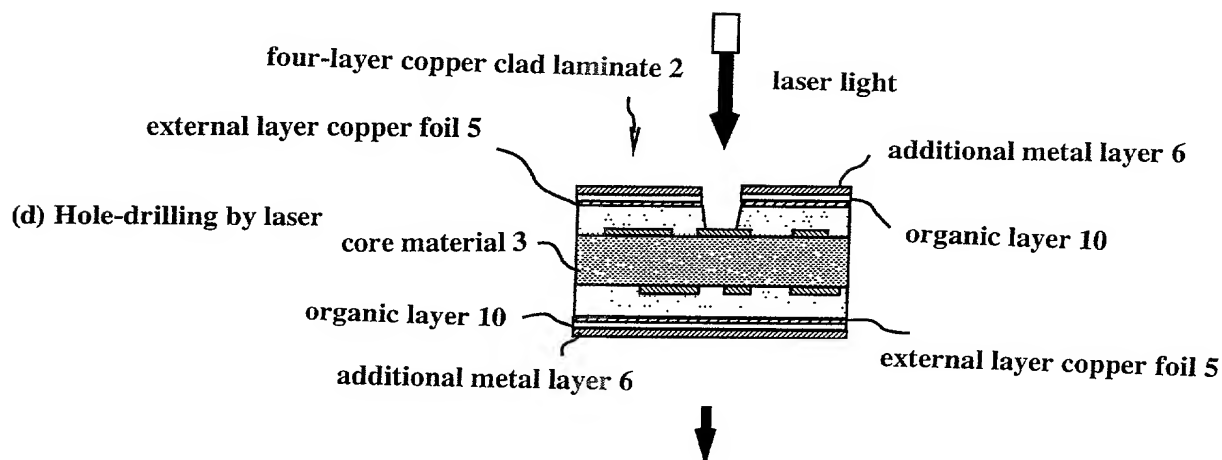
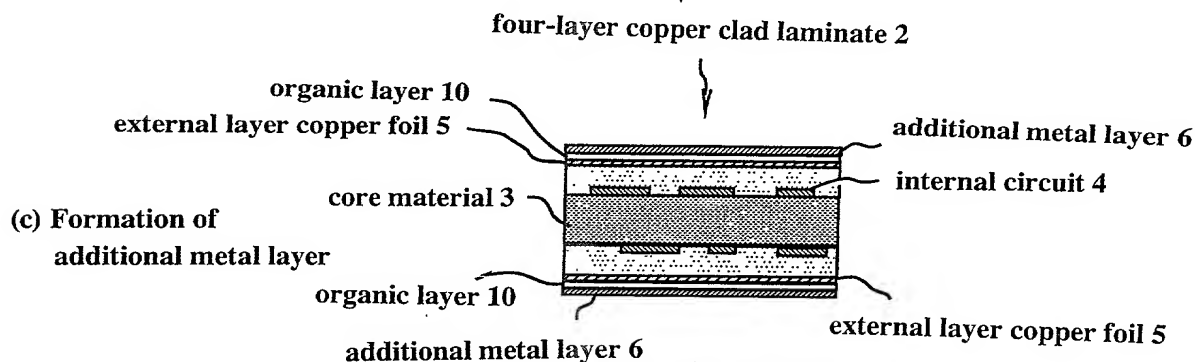
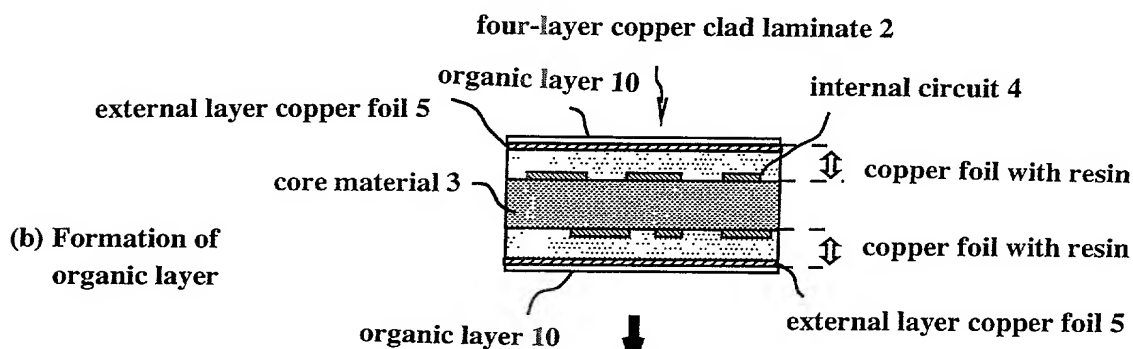
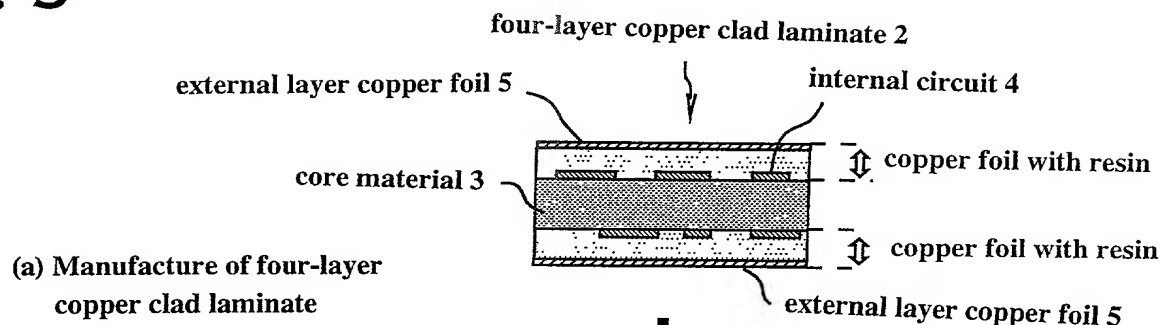


FIG. 10

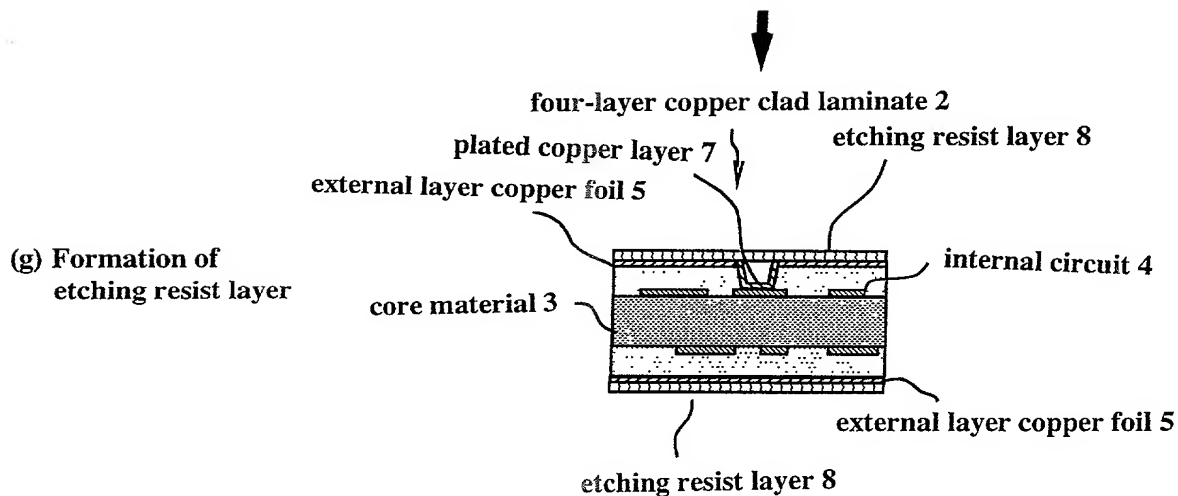
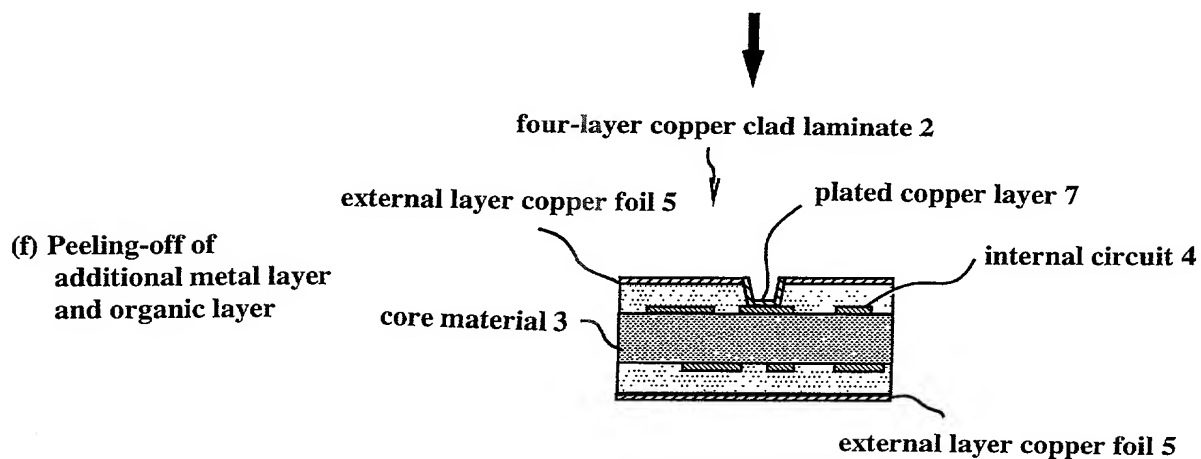
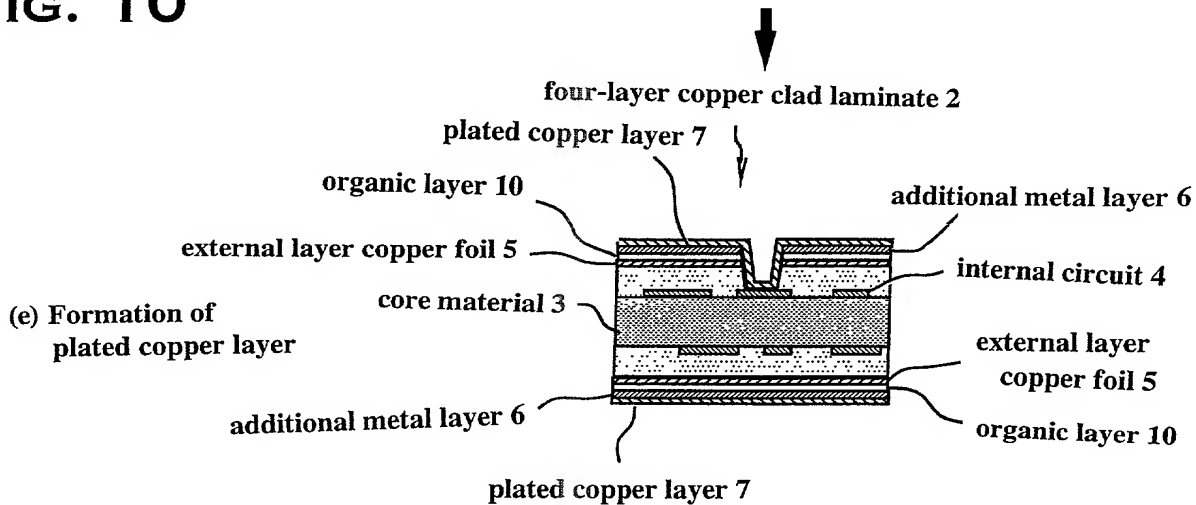


FIG. 11

